

1 (1) TITLE

2 Integrating Chip Scale Packaging Metallization into Integrated Circuit Die  
3 Structures

4 (2) CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is a continuation-in-part of Serial No. 10/453,157, filed June  
6 3, 2003.

7 (3) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR  
8 DEVELOPMENT

9 Not applicable.

10 (4) REFERENCE TO AN APPENDIX

11 Not applicable.

12 (5) BACKGROUND

13 TECHNICAL FIELD

14 [0001] This disclosure relates generally to integrated circuits and, more  
15 particularly to integration of chip-scale packaging input-output bump-  
16 connection metallurgy into integrated circuit structures.

17 DESCRIPTION OF RELATED ART

18 [0002] Semiconductor integrated circuits ("IC") in the state of the art  
19 have been able to pack millions of circuit elements into a relatively  
20 small die, or "chip", e.g., having lateral area footprint, e.g., a 1/4" by  
21 1/4". Most ICs are designed with input-output ("I/O") pads located  
22 along the periphery of the chip; some requiring hundreds of such pads.  
23 These pads are then wire-bonded to connect the IC to the macro-world  
24 of a printed wire board ("PWB"), also known as printed circuit board  
25 ("PCB"), and surrounding discrete elements and other IC electronics on  
26 the board. This conventional perimeter-lead surface mount technology  
27 ("SMT") for complex circuitry with appropriate interconnects often  
28 requires a chip carrier several times greater in size than the chip itself.

1        [0003]                For mobile appliances - e.g., cellular telecommunications  
2                                products, portable digital assistants ("PDA"), notebook computers, and  
3                                the like - or applications where physical space for computers and  
4                                instrumentations is extremely valuable - e.g., aircraft, space shuttles,  
5                                and the like - individual component size and weight are factors which  
6                                are critical to successful design. Thus, there is a conflict between a  
7                                higher density of IC elements on the chip with attendant higher  
8                                input/output ("I/O") needs and a simultaneous demands for continuing  
9                                miniaturization with increased functionality.

10       [0004]                Wafer-level packaging ("WLP"), wherein a single IC die and its  
11                                mounting package are manufactured and tested on a multi-die wafer  
12                                produced by the IC manufacturer prior to singulation into individual  
13                                chips, offers many advantages to the chip manufacturer. One WLP  
14                                solution known in the art is generally referred to in the art as chip-scale  
15                                packages ("CSP"). Chip-scale packaging technology, where the  
16                                peripheral pads are connected to I/O solder balls by a redistribution  
17                                metal layer, provides die-sized packaging, allowing more condensed  
18                                PCB patterns, also referred to in the art as "land patterns" where  
19                                elements have a specific area "footprint."

20       [0005]                Exemplary, conventional, chip-scale technology is demonstrated  
21                                by **FIGURES 1A** and **1B**, taken from Semiconductor International  
22                                magazine, Oct. 2000, pp. 119 - 128, "Wafer-Level Packaging Has  
23                                Arrived," by Dr. Philip Garrou, illustrating the process 100, **FIGURE 1A**,  
24                                and resultant structure 102, **FIGURE 1B**, for chip-scale packaging I/O  
25                                redistribution. As shown in **FIGURE 1A**, "IC" 101 peripheral I/O pads  
26                                103 have an electrical redistribution to I/O bumps 107 via known  
27                                manner processes. Step 100A illustrates the formation of a lower

1 "POLYMER LAYER" 113, FIGURE 1B, (e.g., benzocyclobutene, "BCB"  
2 ) of the chip-scale WLP structure. Step 100B "METALLIZATION"  
3 illustrates an I/O electrical re-distribution for the chip 101 by formation  
4 of traces 109 from pads 103 leading to a centralized region of the chip.  
5 Steps 100C and 100D, "SOLDER MASK," "UBM," respectively, illustrate  
6 the upper polymer layer 113', FIGURE 1B, formation. The process  
7 continues, step 100E, "BUMPS," with an I/O bump formation step  
8 wherein the bumps 107 (e.g., solder balls) are located inwardly from  
9 the chip 101 periphery.

10 [0006] Conductive material (such as a metal, e.g., copper) beams 109  
11 (FIG. 1B) are lithographically defined superjacent the chip passivation  
12 layer 111, e.g., a plasma nitride or the like, generally referred to in the  
13 art as the "topside layer," and within a protective-covering-stress-  
14 absorbing material (e.g., resin, polyimide, or the like) 113, 113',  
15 providing a conventional IC 101. A cross-section of a chip-scale I/O  
16 bump-out packaging structure is shown in FIGURE 1B. A variety of  
17 implementations are described by Garrou. In current wafer-level  
18 packaging, these additional layers of the chip-scale package are  
19 generally so formed on the wafer after the die fabrication is completed,  
20 yielding a plurality of packaged die on the wafer, which has many  
21 advantages for the manufacturer. A thereafter singulated die with chip-  
22 scale package 115 with eight bumps 107 is illustrated in **FIGURE 1C**,  
23 showing that the total footprint is essentially the same as the die area.  
24 The present invention relates to further discoveries in this regard.

25 [0007] While chip-scale packaging has many advantages, it may also  
26 be recognized by those skilled in the art that in the current state-of-the-  
27 art, some die may be too small to accommodate a requisite number of  
28 bumps for the input-output requirements of an underlying chip.

Moreover, in wafer-scale fabrication or for applications which may take advantage of providing a chip-set device including more than one individual die with appropriate interconnections, it would be advantageous to take further advantage of the process steps as shown in FIGURE 1A in constructing appropriate layouts.

[0008] Many publications describe the details of common techniques used in the fabrication of integrated circuits that can be generally employed in the fabrication of complex, three-dimensional, IC structures; see e.g., *Silicon Processes*, Vol. 1-3, copyright 1995, Lattice Press, Lattice Semiconductor Corporation (assignee herein), Hillsboro, Oregon. Moreover, the individual steps of such a process can be performed using commercially available IC fabrication machines. The use of such machines and common fabrication step techniques will be referred to hereinafter as simply: "in a known manner." As specifically helpful to an understanding of the present invention, approximate technical data are disclosed herein based upon current technology; future developments in this art may call for appropriate adjustments as would be apparent to one skilled in the art.

#### (6) BRIEF SUMMARY

[0009] The basic aspects of the invention generally provide for use of chip-scale packaging metallization as part of an integrated circuit active element metallization layer. In an exemplary embodiment, the present invention provides for power MOSFET (metal-oxide-semiconductor-field-effect-transistor) size reduction by including the use of chip-scale metallization as part of the die structure itself.

[0010] In aspect of the invention, an exemplary embodiment is shown as an integrated circuit structure including chip-scale packaging, the structure including: a plurality of active elements in a surface of a

1 semiconductor die; at least one conductive-material bus electrically  
2 interconnecting said active elements; said chip-scale packaging  
3 including at least one, conductive-material, input-output bump  
4 extending outwardly from said die for electrically connecting said  
5 plurality of active elements to off-die electronics, and a beam of  
6 conductive material connecting said bus to said bump; and said bus  
7 having a construction wherein the conductive material forming said  
8 beam is extended to regions of said structure for thickening of said bus  
9 such that resistance of said bus is reduced.

10 [0011] In another aspect of the invention, an exemplary embodiment is  
11 shown as a power MOSFET array integrated circuit device including:  
12 at least a first row of drain regions in a semiconductor surface; at least  
13 a second row of source regions in said surface; channel regions in said  
14 surface, separating source regions of said second row from respective  
15 drain regions of said first row; a gate structure superjacent respective  
16 said channel regions; a first conductive trace for electrically coupling  
17 said drain regions to a first input-output pad; a second conductive trace  
18 for electrically coupling said source regions to a second input-output  
19 pad; a first conductive beam for electrically coupling said first input-  
20 output pad to a first input-output chip-scale packaging bump; and a  
21 second conductive beam for electrically coupling said first input-output  
22 pad to a second input-output chip-scale packaging bump, wherein  
23 conductive material forming said first conductive beam is routed onto  
24 and thickens said first conductive trace for reducing resistance thereof,  
25 and conductive material forming said second conductive beam is  
26 routed onto and thickens said second conductive trace for reducing  
27 resistance thereof.

28 [0012] It is another aspect of the present invention to provide a method

1 for improving ( $R_{ON}$ ) \* Area figure-of-merit for an integrated circuit,  
2 including a top metal layer, where  $R_{ON}$  is a predetermined resistance  
3 characteristic and Area is the lateral footprint area of the integrated  
4 circuit, the method including: forming active elements, including said  
5 top metal layer, in and on a first surface a semiconductor substrate;  
6 and forming metal beams for chip-scale packaging input-out bumps  
7 such that metallization of said beams also extends onto said top metal  
8 layer, increasing the thickness thereof.

9 [0013] Another aspect of the present invention provides an integrated  
10 circuit die having an array of MOSFET devices, each having at and  
11 interconnect traces, having individual elements of said devices sharing  
12 a common top metal trace and pad respectively, the die further  
13 including bump out contacts with metal beams for connecting to said  
14 MOSFET elements respectively, the die further comprising: said top  
15 metal trace in contact over a top surface thereof with a respective said  
16 one of said metal beams formed in either a long, narrow, single strip  
17 via juxtaposed with the IC top metal, a first via connecting the metal  
18 down to the top metal as the bump-out metal comes into the IC device  
19 active element regions which extends across the active element  
20 regions to a second via at a distal end or, wherein the MOSFET is an  
21 array broken up into two or more sections having a plurality more tack  
22 down vias therefor.

23 [0014] The foregoing summary is not intended to be inclusive of all  
24 aspects, objects, advantages and features of the present invention nor  
25 should any limitation on the scope of the invention be implied  
26 therefrom. This Brief Summary is provided in accordance with the  
27 mandate of 37 C.F.R. 1.73 and M.P.E.P. 608.01(d) merely to apprise  
28 the public, and more especially those interested in the particular art to

1 which the invention relates, of the nature of the invention in order to be  
2 of assistance in aiding ready understanding of the patent in future  
3 searches.

4 (7) BRIEF DESCRIPTION OF THE DRAWINGS

5 [0015] FIGURE 1A (Conventional) is a schematic chip-scale process  
6 flow diagram.

7 [0016] FIGURE 1B (Conventional) is a partial cross section, elevation  
8 view, of a chip-scale I/O redistribution die formed in accordance with  
9 the process as shown in FIGURE 1A.

10 [0017] FIGURE 1C (Conventional) is a schematic perspective view of a  
11 singulated wafer-level chip-scale package and attached die resultant  
12 from a process and fabrication as shown in FIGURES 1A and 1B.

13 [0018] FIGURE 2A in accordance with a first exemplary embodiment of  
14 the present invention is a schematic IC layout view for a simplified  
15 power MOSFET array.

16 [0019] FIGURE 2B is an elevation view for a partial cross section of the  
17 structure as shown in FIGURE 2A.

18 [0020] FIGURE 3A is a plan view (overhead) schematic illustration of a  
19 region of a semiconductor wafer, showing two complete and two  
20 cutaway integrated circuit dice wherein a chip-scale interconnect is  
21 incorporated between die.

22 [0021] FIGURE 3B is an elevation view projection of the schematic  
23 illustration of FIGURE 3A.

24 [0022] Like reference designations represent like features throughout  
25 the drawings. The drawings in this specification should be understood  
26 as not being drawn to scale unless specifically annotated as such.

27 (8) DETAILED DESCRIPTION

28 [0023] To simplify the description of the present invention, a simplified

1 embodiment of an IC structure comprising an array of power MOSFETs  
2 is used. No limitation on the scope of the invention is intended by the  
3 inventors in using this simple device example, nor should any be  
4 implied therefrom. Those skilled in the art will recognize that the basic  
5 methodology of this described technology can be extended to most  
6 types of die, having other active elements besides MOSFET elements -  
7 e.g., emitter and collector pairs of bipolar transistors, anode/cathode  
8 pairs, diode poles, programmable logic arrays elements, and the like -  
9 which are amenable to chip-scale packaging and where a PIE  
10 characteristic is definable.

11 [0024]

As set forth in the Background section hereinabove,  
12 miniaturization of ICs is a continuing goal; chip-scale packaging is a  
13 technology in furtherance of this goal. One measure-of-performance,  
14 or figure-of-merit, for power MOSFET ICs, having a given operating  
15 voltage, is to have a lowest possible " $(R_{ON}) * \text{Area}$ " product in  
16 milliohms-mils<sup>2</sup>. That figure-of-merit is also referred to hereinafter as  
17 PowerFET Interconnect Efficiency ("PIE"). However, it is recognized  
18 that for power MOSFET chip designs there is a true PIE characteristic  
19 reflecting the difference between an ideal test pattern, defining 100%  
20 efficiency, and losses induced inherently by silicon implementation and  
21 packaging result in a PIE in the approximate range of 50% - 75%.  
22 Much of the loss in efficiency may be attributable to the metal electrical  
23 traces running to I/O pads and particularly to the wire-bonds used in  
24 SMT packaging. The use of CSP packaging therefore eliminates the  
25 wire-bonds provides one improvement in the PIE characteristic by  
26 decreasing the  $R_{ON}$  factor for a given chip footprint. Simply increasing  
27 each buses thickness during die fabrication to reduce  $R_{ON}$  itself for a  
28 given chip footprint is complex, e.g., requiring added steps such as



electro-less plating. The present invention improves the state of the art by using CSP technology to lower the PIE characteristic for a chip, and further, where desirable for miniaturization, to reduce the footprint for a given PIE value.

[0025] FIGURE 2A, a partial device layout view, schematically illustrates a simplified MOSFET array IC device 201 comprising standard power MOSFETs 203, having respective source 205, "S," and drain 207, "D," regions. A gate structure 209 overlays the channel region between each source 205 and drain 207 of each MOSFET 203. Contacts 211<sub>s</sub>, 211<sub>D</sub> to each respective source 205 and drain 207 are provided for connecting metal traces 212<sub>s</sub>, 212<sub>D</sub> to I/O pads 213<sub>s</sub>, 213<sub>D</sub> for the respective source/drain regions. It will be recognized that in many implementations, the sources 205 are a continuous strip and the drains 207 are a continuous strip. Note here, that in alternative IC embodiments, these source/drain metal traces may be, in fact, any top metal layer - commonly referred to in the art as "Metal 1," "Metal 2," "Metal 3," et seq., depending on the specific IC functionality and I/O requirements of particular elements of the chip's active devices.

[0026] Turning also to **FIGURE 2B**, a schematic elevation view of device 201 through plane A- -A of FIGURE 2A is provided. The illustration is of a cross-section through separate drain regions, but again, in other implementations, those regions may be a continuous strip. In terms of the prior art, it is known that a passivation material normally overlays the metal traces 212<sub>s,D</sub>. Looking also back to FIGURE 1B, it should be recognized that the pad 103 there is equivalent to a pad 213<sub>s,D</sub> in accordance with the present invention as shown in FIGURES 2A and 2B. Conventionally, next, a chip-scale metal beam 109 used for the pad-to-bump redistribution to I/O bump

107 of FIGURE 1B would be formed so as to be embedded in the protective-covering-stress-absorbing material 113. Another via would be required above the pad 103 to bring the metal beam 109 down to the pad 103.

[0027] Now however, referring back to FIGURES 2A and 2B, in order to improve PIE in accordance with the present invention, in redistribution of an I/O pad  $213_{s,D}$  to a bump 107 (pseudo-isometrically shown in FIGURE 2B), metal traces  $212_{s,D}$  are opened, respectively, to  $Via_2$  by appropriate masking and etching, or other in a known manner, in a geometry wherein the formation of the beam 109 also deposits metal 109' on the associated trace. Remember  $Via_2$  was conventionally used only for the pad-to-bump interconnect as shown in FIGURE 1B, but now  $Via_2$  for each respective region is also open, forming a slot or trench, across the top surface of the already formed metal trace  $212_{s,D}$  comprising respective source and drain interconnects. Therefore, deposition, or reflow, of the heretofore CSP metal - as in step 105, "Metallization," of the Redistribution Process Flow of FIGURE 1A - to form what in FIGURE 1B is only an encapsulated beam 109 from the I/O pad 103 out to the bump 107, now also lays the same metal 109', FIGURE 2B, superjacent to the source/drain metal  $212_{s,D}$ . In this manner, the first metallization of the I/O redistribution process is combined with the conventional Pad Mask step of die fabrication.

[0028] In other words, the masking and metallization steps are modified so that rather than merely being formation of the redistribution beam 109 from a pad 213 to an associated bump 107, the metal 109, 109' also forms superjacent an exposed surface of the top metal 212 of the device as shown in FIGURE 2B. This effectively increases the thickness of the metal traces  $212_{s,D}$ . Increasing the thickness of the

1 metal traces reduces the resistance, therefore enhancing the electrical  
2 current capability, and therefore lowers PIE for the same die area for a  
3 given IC operating voltage. Depending on the specific implementation  
4 and IC design in accordance with the present invention, it has been  
5 determined that the ( $R_{ON}$ ) \* Area product may be improved by a factor  
6 in the range of approximately 10-30%.

7 [0029] There are at least three fundamental fabrication process  
8 techniques for having the bump-out metal 109, 109' also be in direct  
9 contact with the IC top metal 212 to achieve this structure. First, a  
10 long, narrow, single strip via juxtaposed with the IC top metal may be  
11 provided. Second, a first Via connecting the metal down to the top  
12 metal as the bump-out metal comes into the IC device active element  
13 regions, which then stretches across the active element regions to a  
14 second via at a distal end. Third, similar to the second, except wherein  
15 the device transistor array is broken up into two or more sections to  
16 allow more tack down vias. The first is preferred where the element  
17 array is wide enough to support a single, long, narrow via. Thus, it  
18 should be recognized by those skilled in the art that a variety of  
19 implementations may be constructed in accordance with the need of  
20 any specific IC design.

21 [0030] Moreover, looking a complementary aspect of the present  
22 invention, if the current  $R_{ON}$  is an acceptable operational design  
23 specification, conventional die shrink technology may be employed to  
24 reduce the die footprint. In other words, for a predetermined  
25 specification for  $R_{ON}$ , lateral footprint area of said structure may be  
26 reduced by a factor in the range of approximately 10-30%.

27 [0031] The possibility of modifications and variations for other types of  
28 integrated circuits, discrete devices, logic devices, thin-film resistor

1 arrays, and the like, will be apparent to practitioners skilled in the art.  
2 Clearly, a variety of specific geometric arrangements for the beams  
3 and overlay of beam metal onto the top metal can be tailored for each  
4 implementation.

5 [0032] Turning now to FIGURES 3A and 3B, an exemplary embodiment  
6 of a method and structure for using chip-scale process to interconnect  
7 a plurality of chips together is demonstrated. Such a method and  
8 structure provides an advantage of allowing semi-customization of chip  
9 sets. For example, if a wafer is fabricated having very small individual  
10 die - - for example, a relatively simple, smart switch IC device - - where  
11 the single die is too small for four chip-scale I/O bumps, using existing  
12 tooling and incorporating chip-scale metallization as described herein,  
13 it would be possible to interconnect sets of the chips, e.g., four in  
14 parallel, putting one bump on each die. Various such implementations  
15 can be envisioned. Another embodiment is described with respect to  
16 FIGURES 3A and 3B.

17 [0033] As seen from an overhead view in FIGURE 3A, at the wafer  
18 fabrication level, a plurality of die 301, "Die #1" 301A and "Die #2"  
19 301B being shown in substantially complete form, are formed in and on  
20 a wafer 302. In the normal course of chip manufacture, the region 304  
21 between each chip 301 is where scribe lines, illustrated by line 306,  
22 are formed for separating the die into individual dice for further  
23 packaging. Normally, a chip passivation layer 308, e.g., a nitride, is  
24 absent in the scribe line regions 304.

25 [0034] However, it is known in the art to manufacture chip-sets  
26 composed of a plurality of chips which are conventionally separated  
27 from the wafer, repackaged, mounted on circuit boards and  
28 interconnected appropriately. As an exemplary implementation,

1 assume Die #1 301A is a booster switch IC device and Die #2 301B is  
2 a Schottky diode IC device to prevent an over-voltage feedback into  
3 the switch; the two chips 301A, 301B are therefore to be  
4 interconnected as a chip-set.

5 [0035] As described hereinabove with respect to FIGURES 1B, 1C, 2A  
6 and 2B, fabricating a chip-scale type packaged chip 102, 115, 201,  
7 respectively, with I/O bumps 107, 207, 107<sub>x</sub>, respectively, in  
8 accordance with the present invention, one can make use of the bump  
9 beams 109, 109' as top-most metal layer for the integrated circuit itself.  
10 For manufacture of discrete chips, it is conventional to mask off the  
11 wafer to eliminate the formation in the scribe line regions 304 of  
12 passivation 308 between dice. In chip-scale fabrication, a person  
13 skilled in the art would also in like manner eliminate the formation of  
14 chip-scale passivation material 111 and chip-scale polyimide material  
15 113, FIGURE 1B in the scribe line regions 304. However, in  
16 accordance with the present invention and this exemplary embodiment  
17 of FIGURES 3A and 3B, for chip-scale fabrication, the polyimide-like  
18 (preferably benzocyclobutene, "BCB") layers "BCB1" 311 and "BCB2"  
19 313 between die 301A, 301B which are to be electrically  
20 interconnected are not eliminated between die to be interconnected, in  
21 this example at respective chip component bumps 307<sub>3</sub>, 307<sub>8</sub>.

22 [0036] In the fabrication process in accordance with the present  
23 invention, when the first chip-scale polyimide-like layer 311 is formed,  
24 the mask is appropriately left open according to a predetermined  
25 design between the die 301A, 301B to be interconnected in order for a  
26 polyimide-like bridge 311BR, FIGURE 3B, to be formed where the  
27 electrical interconnect is needed between die. In other words, after the  
28 active components (not shown) of each IC 301 are formed with

1 individual chip passivation layer 308 and pad contacts superjacent a  
2 top surface 305 of the wafer and chips therein, the subsequent mask  
3 step for forming the polyimide-like 309 for the chip-scale bump-out  
4 structure is used for form appropriate polyimide-like bridges 309BR  
5 between chips in accordance with the specific implementation design.  
6 It is an advantage of the present invention that polyimide-like material  
7 will flow well over the known layer elements, alignment markers, and  
8 the like, in the scribe line region 304.

9 [0037] As can be recalled with respect to FIGURE 1A, the redistribution  
10 "metallization" creates the interconnect beams 109, FIGURE 1B,  
11 between each chip I/O pad 103 and its associated bump 107.  
12 Returning to FIGURES 3A and 3B, with the polyimide-like bridge  
13 311BR left between predetermined bumps 307<sub>3</sub>, 307<sub>8</sub> on different die  
14 301A, 301B, respectively, when the top metal layer and bump beams  
15 309 are formed to connect associated chip pads 303 and bumps 307,  
16 the ReDistributed Layer (RDL) metal will also flow across the scribe  
17 line region 304 between associated dice 301A, 301B, forming an  
18 electrical interconnect 309BR.

19 [0038] Thus, in accordance with the present invention, the I/O bumps  
20 107, 207, 307 which act as electrical interconnection terminals for  
21 discrete chips and the process used in forming the bumps are now  
22 employed for interconnecting chips during wafer fabrication. It can also  
23 be recognized that the same concept is applicable to system-scale chip  
24 sets and wafer-scale integrated circuit devices. Concomitant formation  
25 of the bump beams 309 and inter-die electrical bridges 309BR provides  
26 simplicity in creating a wafer-level fabrication mask-set.

1 [0039] The foregoing Detailed Description of exemplary and preferred  
2 embodiments is presented for purposes of illustration and disclosure in  
3 accordance with the requirements of the law. It is not intended to be  
4 exhaustive nor to limit the invention to the precise form(s) described,  
5 but only to enable others skilled in the art to understand how the  
6 invention may be suited for a particular use or implementation. No  
7 limitation is intended by the description of exemplary embodiments  
8 which may have included tolerances, feature dimensions, specific  
9 operating conditions, engineering specifications, or the like, and which  
10 may vary between implementations or with changes to the state of the  
11 art, and no limitation should be implied therefrom. Applicant has made  
12 this disclosure with respect to the current state of the art, but also  
13 contemplates advancements during the term of the patent, and that  
14 adaptations in the future may take into consideration those  
15 advancements, in other word adaptations in accordance with the then  
16 current state of the art. It is intended that the scope of the invention be  
17 defined by the Claims as written and equivalents as applicable.  
18 Reference to a claim element in the singular is not intended to mean  
19 "one and only one" unless explicitly so stated. Moreover, no element,  
20 component, nor method or process step in this disclosure is intended to  
21 be dedicated to the public regardless of whether the element,  
22 component, or step is explicitly recited in the Claims. No claim element  
23 herein is to be construed under the provisions of 35 U.S.C. Sec. 112,  
24 sixth paragraph, unless the element is expressly recited using the  
25 phrase "means for. . ." and no method or process step herein is to be  
26 construed under those provisions unless the step, or steps, are  
27 expressly recited using the phrase "comprising the step(s) of. . ."  
28 What is claimed is: